

REV	REVISIONS DESCRIPTION	DATE	APPROVED
1	ENG DEL PER ERC # E0260L	1/3/84	<i>[Signature]</i>

ENVIRONMENTAL/RELIABILITY ENGINEERING

5100 DESIGN VALIDATION

TEST PLAN

ENGINEERING RELEASED



		DRAWN BY	DATE	 Atari, Inc. 30 E. Plumaria Drive San Jose, CA 95134  A Warner Communications Company					
NEXT ASSY	USED ON	CHECKED							
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				APPROVED <i>[Signature]</i> Dec. 21, 1983	SIZE A	DRAWING NO.	C024673- 130	REV	1
				APPROVED <i>Kleber</i> 12/21/83	SCALE	SHEET	1	OF	10

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1.0 PURPOSE

The Design Validation Test Plan Task is to define the prototype tests to be conducted and provide capability for verifying conformance to the 5100 test specification.

2.0 SCOPE

This test plan shall apply to all lab and production prototype 5100 units being submitted for test.

3.0 REFERENCES

1. C024142 ATARI CX5100 Test Specification
2. C0-24673-131 ATARI CX5100 Reliability Guidelines
3. C0-61616 ATARI Environmental Engineering Manual
4. C021703 ESD Sensitivity Specification
Product Level

4.0 ENVIRONMENTAL TESTS

All tests will comply with the Environmental Engineering Manual except as noted. The following tests are to be performed with no damage imparted to the 5100. All functional specifications of the 5100 will remain applicable.

1. Storage mode (non-operating) thermal shock per Atari Specification Environmental Engineering Manual C061616, Revision A.
2. Operating mode (Thermal Cycling) per Atari Specification Environmental Engineering Manual C061616, Rev. A.
3. Temperature and Humidity. The 5100 will be subject to the following temperature and humidity extremes:

Operational Mode

Maximum: 80% R.H. (@ 10 degrees C and 40 degrees C:
One hour minimum @ each temperature.)

Minimum: 20% R.H. (@ 10 degrees C and 40 degrees C:
One hour minimum @ each temperature.)



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Storage Mode

Maximum: 90% R.H. (@ 10 degrees C and 55 degrees C:
One hour minimum @ each temperature.)

Minimum: 10% R.H. (@ -20 degrees C and 55 degrees C:
One hour minimum at each temperature.)

4. Mechanical Shock and Vibration (unpackaged) per Atari Specification Environmental Engineering Manual C061616, Revision A.

5. EMI

The 5100 will meet with any compliances that are required. These will include the following: UL 114 and 94HB, CSA C22.2 No. 154, FCC Docket 20780, Part 15, Subpart I and J, Class B and Part 68.

6. ESD

The 5100 will be subjected to the following electrostatic discharge test: External surfaces are subjected to at least 50 discharges up to 25KV from a 100pf capacitor through a 1,500 ohm resistance. No physical damage to the 5100 is allowed. (ESD sensitivity specification/product level, C021703.)

7. PACKAGE TESTS (PER ENVIRONMENTAL ENGINEERING MANUAL C061616, REV. A.)

The 5100 packaging will undergo the following tests:

Package Vibration: This will include a secured and non-secured package vibration test. This will be used to determine the ability of the packing to protect the product during shipping and handling.

Package Drop: The packaging will be subjected to twelve drops. These will be on six faces, four edges and two corners from a height appropriate to the packout weight per NSTA specification.

5.0 FUNCTIONAL TESTING

The prime references for this testing will be the 5100 Functional Test Specification and the Reliability Guidelines.



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Test and verify the following:

1. Power Supply Adaptor will be verified to comply with the test specification and the following. Power Adaptor A.C. input and D.C. output under full load of 1 AMP for compliance is:

<u>Input</u>	<u>Output</u>
o Low line (108VAC) @ 60 HZ	8.2VDC \pm 5%; 1 AMP \pm 5%
o Normal line (120VAC) @ 60HZ	9.9VDC \pm 5%; 1 AMP \pm 5%
o High Line (132VAC) @ 60 HZ	11.6VDC \pm 5%, 1 AMP \pm 5%

NOTE: Maximum input power T.B.D.

2. Thermal Mapping

Monitor, for conformance to specifications, critical ICs, including linear devices, passive components, etc.

3. Controller Ports

Controller ports will be verified to comply with all Atari controller products per test specification requirements.

4. RF Output

The RF modulator output will be verified to comply with the test specification.

5. Cartridge Interface

o Verify all pinouts as to conformance to test specification requirements.

o Utilize test cartridge, or equivalent, to verify conformance when running environmental tests.

6. Timing

The prime timing concerns are the D-RAM read/write cycles.



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6.1 AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Time Between Refresh	tREF		4	ms
Random Read/Write Cycle Time	tRC	330		ns
Delay Time $\overline{\text{CAS}}$ HIGH to $\overline{\text{RAS}}$ LOW	tCRP	25		ns
Access Time from $\overline{\text{RAS}}$	tIAC		200	ns
Access Time from $\overline{\text{CAS}}$	tCAC		120	ns
Transition Time	tT	3	50	ns
$\overline{\text{RAS}}$ Precharge Time	tRP	120		ns
$\overline{\text{RAS}}$ Pulse Width	tRAS	200	10000	ns
$\overline{\text{RAS}}$ Hold Time After $\overline{\text{CAS}}$ LOW	tRSH	120		ns
$\overline{\text{CAS}}$ Precharge Time	tCPN	45		ns
$\overline{\text{CAS}}$ Pulse Width	tCAS	120	10,000	ns
$\overline{\text{CAS}}$ Hold Time After $\overline{\text{RAS}}$ LOW	tGSH	200		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	tRCD	30	100	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Set Up Time	tCRP	25		ns
Row Address Set Up Time	tASR	0		ns
Row Address Hold Time	tRAH	25		ns
Column Address Set Up Time	tASC	0		ns
Column Address Hold Time After $\overline{\text{CAS}}$ LOW	tCAH	50		ns
Read Command Set Up Time Referenced to $\overline{\text{CAS}}$	tRCS	0		ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	tRRH	20		ns
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	tRCH	0		ns
Write Command Hold Time After $\overline{\text{CAS}}$ LOW	tWCH	80		ns
Write Command Pulse Width	tWP	55		ns
Write Command to $\overline{\text{RAS}}$ Lead Time	tRWL	80		ns



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6.1 CONTINUED

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Command to $\overline{\text{CAS}}$ Lead Time	tCWL	80		ns
Data In Set Up Time	tDS	0		ns
Data In Hold Time After $\overline{\text{CAS}}$ LOW	tDH	80		ns
Access Time from $\overline{\text{OE}}$	tOEA		50	ns
$\overline{\text{OE}}$ to Data In Delay Time	tOED	50		ns
Output Buffer Turn Off Delay from $\overline{\text{OE}}$	tOEZ	0	40	ns
Output Buffer Turn Off Delay from $\overline{\text{CAS}}$	tOFF	0	50	ns



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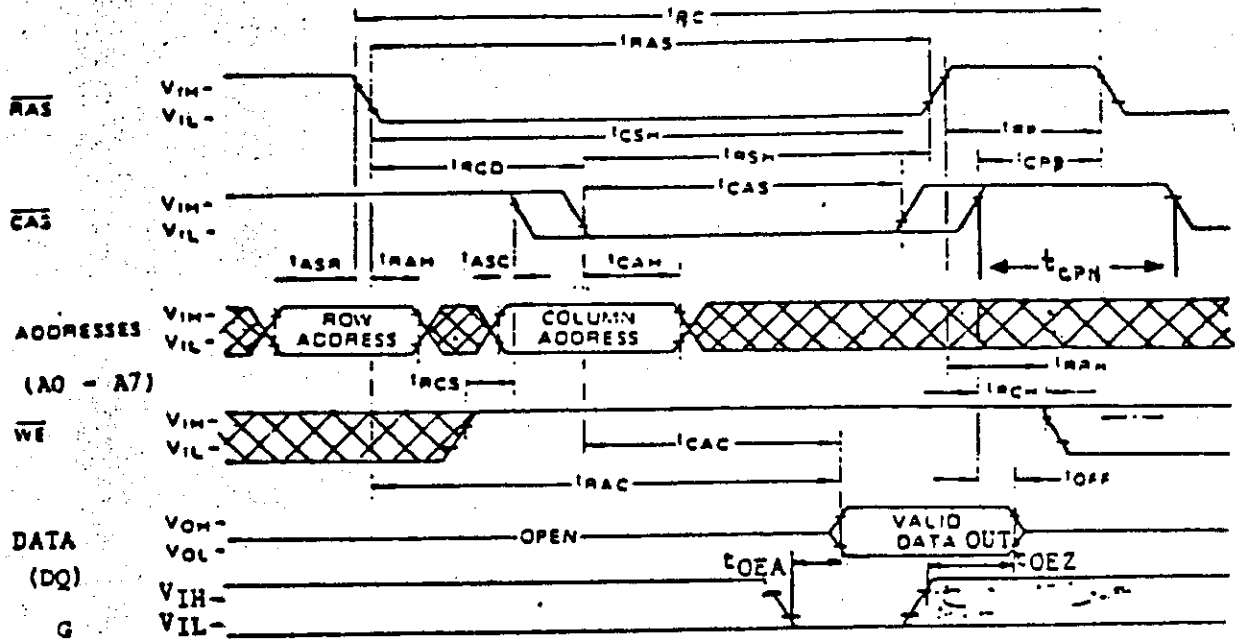
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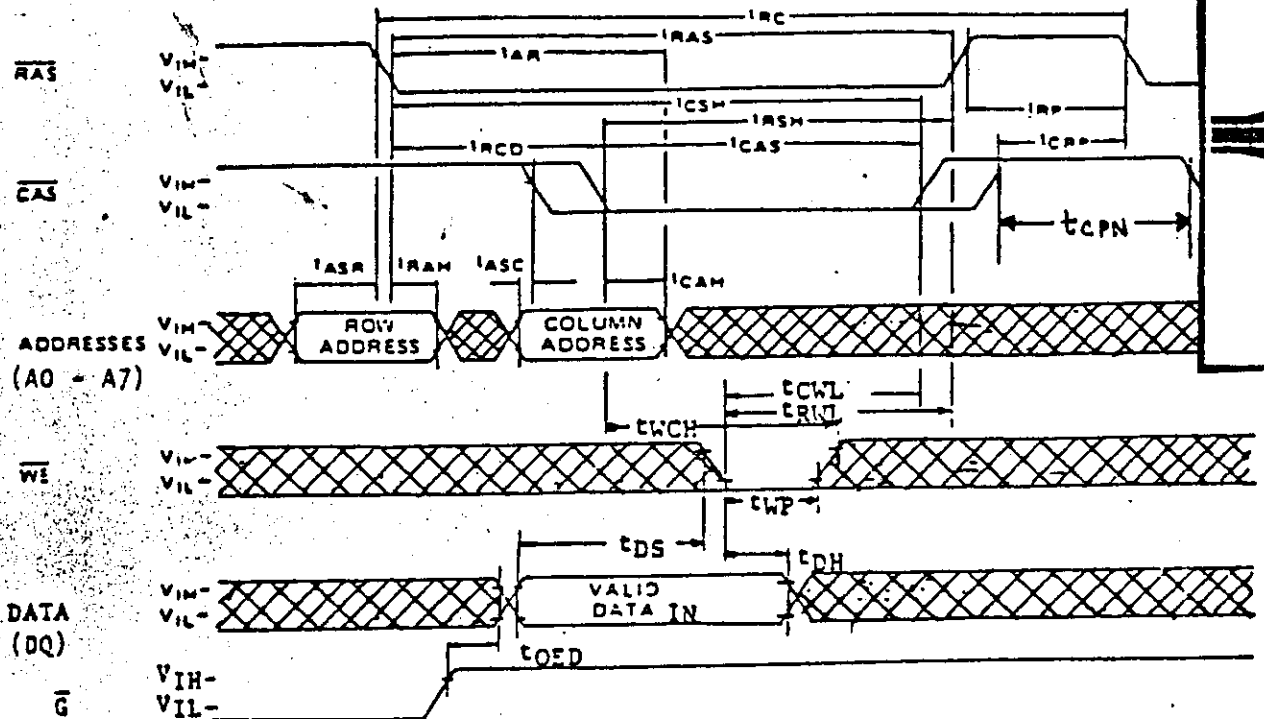
READ CYCLE TIMING

NOTE: RISE AND FALL TIMES ARE MEASURED AT 10% AND 90% OF THE WAVEFORM MAXIMUM AMPLITUDE.



WRITE CYCLE TIMING

NOTE: RISE AND FALL TIMES ARE MEASURED AT 10% AND 90% OF THE WAVEFORM MAXIMUM AMPLITUDE.



⊠ DON'T CARE: INCLUDES ANY STATIC LEVELS OR TRANSIENTS BETWEEN THE HIGH AND LOW LOGIC LEVELS.

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7. Software Testing and Validation

Complete software regression testing will be done with the existing and new interfaces, operating system, and cartridges to determine conformance to the software external reference specifications portion of the functional specification. (All 5200 cartridges must function with 5100 console.)

6.0 SAFETY

The 5100 product must comply and be verified to all Atari Engineering product specifications and Corporate Product Safety requirements. In the event of a conflict with any other document, vendor/manufacturer is responsible to notify Atari Engineering and Corporate Product Safety of the conflict for written disposition from Atari, Inc.

7.0 MECHANICAL CHARACTERIZATION AND LIFE TESTS

1. Mechanical Characterization: Each unit will be fully reviewed for conformance to Engineering product and quality specifications.
2. Mechanical Life: Utilizing special exerciser fixtures, all moving parts will be operated on a continuous basis while outputs are monitored. Purpose of this test is to determine life expectancy of mechanical parts. Failing parts will be replaced and test continued. Number of actuations (or time) will be logged on each failure along with amount of time required to repair or replace the failed part.

8.0 DOCUMENTATION

Detailed logs and charts will be maintained during every test listing, test number, unit number, test condition, time measurement and recommendations.

Failure data will also include the following:

- o Number of DC Parametric failures
- o Number of functional failures
- o Number of catastrophic failures



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9.0 TEST RESPONSIBILITIES

Corporate Product Safety
 Design Eng. Hardware Software

Env./Rel. Engineering
 Transfer Engineering

Item	Env./Rel. Engineering	Transfer Engineering	Design Eng. Hardware Software	Corporate Product Safety
All Environmental Tests Less EMI	X			
EMI		X		
Functional Testing	X		X	
Safety	X	X	X	X
Mechanical Characterization and Life Tests	X			
Documentation	X	X	X	X



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