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<th>REVISIONS DESCRIPTION</th>
<th>DATE</th>
<th>APPROVED</th>
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<td>3</td>
<td>ENG REL PER ERC # EQ LD4D</td>
<td>4/3/84</td>
<td>47</td>
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<td>4</td>
<td>INCORPORATED PER ERC E0481</td>
<td>4/5/84</td>
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</tr>
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**ENGINEERING RELEASED**

**DRAWN BY**

**DATE**

**CHECKED**

**ENGINEER**

**APPROVED**

**TITLE**

**SIZE**

**DRAWING NO.**

**SCALE**

**SHEET 1 OF 14**

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12.0 ELECTRICAL CHARACTERIZATION TESTING
13.0 Pin Assignment
1.0 **SCOPE**

This document is a preliminary specification of the electrical and mechanical requirements for a 40 pin custom high speed CMOS gate array I.C. device designated for use on the "TONG" project. The device is currently under development and there may be revisions to this document before it is Production Released.

2.0 **APPLICABLE DOCUMENTS**

The following documents, at the revision which is in effect on the date of the Purchase Order, shall form part of this specification to the extent referenced herein.

a. CO99901 - Qualification and Reliability Requirements for Integrated Circuits and Discrete Semiconductors.

b. CO99902 - Handling of Devices Susceptible to Static Discharge.

c. CO99905 - External Visual and Solderability Requirements.

d. CO99906 - Internal Visual Requirements for Atari Semiconductors.

e. CO21538 - Electrostatic Discharge Sensitivity Testing.

f. CO99931 - Dual In-Line Package, General Specifications.

3.0 **DEVIATIONS**

Product sold to Atari, Inc. under this specification must be identical to original approved samples. Any changes to the product must receive Atari, Inc. sample reapproval prior to delivery. Any deviation from this specification, or from any of the above listed applicable documents, must be approved in writing through the current Atari Deviation Procedure prior to any deviation taking place.

4.0 **PRECEDENCE**

This specification, including all approved deviations, shall be the governing document for device acceptance. In the event of conflict between this document and any other document, contract, specification or requirement, the manufacturer is responsible to notify Atari, Inc. for written disposition from the affected functional group(s), as identified within this document.

5.0 **GENERAL REQUIREMENTS**

5.1 **ELECTROSTATIC DISCHARGE**

Parts must conform to the requirements of the Atari, Inc. Specification #CO21538, Electrostatic Discharge Sensitivity Testing.
5.2 MARKING

Minimally, parts must be marked permanently and legibly as per Atari, Inc. Specification #CO99901 para. 10.1.12 with:

a. Atari Part Number
b. Date Code
c. Copyright Symbol and information:
   - © ATARI (Year); year must be represented as either the full
     year (e.g. 1983) or the last two digits (e.g. 83)
d. Vendor or industry recognized identification symbol
e. Pin #1 Identification

5.3 BLOCK DIAGRAM

```
<table>
<thead>
<tr>
<th>INPUTS</th>
<th>VCC</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A8-A15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROMEN</td>
<td></td>
<td>/S4</td>
</tr>
<tr>
<td>BASICEN</td>
<td></td>
<td>/S5</td>
</tr>
<tr>
<td>READ/(WRITE)</td>
<td></td>
<td>/BASIC</td>
</tr>
<tr>
<td>/REF</td>
<td></td>
<td>/OS</td>
</tr>
<tr>
<td>/INTMPE</td>
<td></td>
<td>/CCNTL</td>
</tr>
<tr>
<td>/HANDLER</td>
<td></td>
<td>/PIA</td>
</tr>
<tr>
<td>RD4, RD5</td>
<td></td>
<td>/POKEY</td>
</tr>
<tr>
<td>MAP</td>
<td></td>
<td>/GTIA</td>
</tr>
<tr>
<td>/D1CFRD</td>
<td></td>
<td>/RAMINH (EXTENB)</td>
</tr>
<tr>
<td>/AC1AIROQ</td>
<td></td>
<td>/DBUSEN</td>
</tr>
<tr>
<td>DISKBUSY</td>
<td></td>
<td>D0</td>
</tr>
<tr>
<td>/SCQ2ARQ</td>
<td></td>
<td>D1</td>
</tr>
<tr>
<td>/EXTSEL</td>
<td></td>
<td>D7</td>
</tr>
<tr>
<td>CLK2</td>
<td></td>
<td>BREAD/(WRITE)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>/PBIIDATEN</td>
</tr>
</tbody>
</table>

VSS
```

NOTE: See Section 13.0 for pin assignment.
5.4 PACKAGE DESCRIPTION

Package shall be void-free plastic.

5.5 LEAD INTEGRITY AND SOLDERABILITY

As per Atari, Inc. Specification #CO99901, para. 10.1.11 Lead Integrity and 10.1.16 Solderability.
6.0 **ABSOLUTE MAXIMUM RATINGS**

Limits beyond which the life of the part may be impaired. It is **NOT** implied that the device should be operated at these limits. If the part is operated at or near these limits, applicable manufacturers' derating calculations must be imposed.

<table>
<thead>
<tr>
<th>ITEM</th>
<th>CHARACTERISTIC</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>SUPPLY VOLTAGE Vcc TO GND (Vcc)</td>
<td>-0.5 TO +7.0</td>
<td>V</td>
</tr>
<tr>
<td>6.2</td>
<td>VOLTAGE APPLIED TO ANY INPUT (Vai)</td>
<td>-0.5 TO +7.0</td>
<td>V</td>
</tr>
<tr>
<td>6.3</td>
<td>VOLTAGE APPLIED TO ANY OUTPUT (Vao)</td>
<td>-0.5 TO +7.0</td>
<td>V</td>
</tr>
<tr>
<td>6.4</td>
<td>POWER DISSIPATION (Pd)</td>
<td>75</td>
<td>mW</td>
</tr>
<tr>
<td>6.5</td>
<td>JUNCTION TEMP. Ta=70° (Tj)</td>
<td>TBD</td>
<td>°C</td>
</tr>
<tr>
<td>6.6</td>
<td>OPERATING TEMPERATURE (Ta)</td>
<td>0 TO 70</td>
<td>°C</td>
</tr>
<tr>
<td>6.7</td>
<td>STORAGE TEMPERATURE (Tst,j)</td>
<td>-55 TO +150</td>
<td>°C</td>
</tr>
</tbody>
</table>
7.0 **STATIC CHARACTERISTICS**

Unless otherwise specified:

a. $0 \leq T_a \leq 70^\circ C$

b. $4.75 \leq V_{cc} \leq 5.25$

c. Positive current flows into the device

d. $C_{LOAD} = 50\text{pF}$

<table>
<thead>
<tr>
<th>ITEM</th>
<th>CHARACTERISTICS</th>
<th>CONDITION</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.1</td>
<td>INPUT VOLTAGE HIGH (VIH)</td>
<td></td>
<td>2.0 $V_{cc}$</td>
<td>V</td>
</tr>
<tr>
<td>7.2</td>
<td>INPUT VOLTAGE LOW (VIL)</td>
<td></td>
<td>-0.3 0.8</td>
<td>V</td>
</tr>
<tr>
<td>7.3</td>
<td>INPUT CURRENT ($I_I$)</td>
<td>$0 \leq V_{in} \leq 5.25$ $V_{cc} = 5.25$</td>
<td>-10 10</td>
<td>uA</td>
</tr>
<tr>
<td>7.4</td>
<td>OUTPUT VOLTAGE HIGH (VOH)</td>
<td>$V_{cc} = 4.75$ $I_{OH} = -100\mu A$</td>
<td>2.4 5.0</td>
<td>V</td>
</tr>
<tr>
<td>7.5</td>
<td>OUTPUT VOLTAGE LOW (VOL)</td>
<td>$V_{cc} = 4.75$ $I_{OL} = 1.6 \text{mA}$</td>
<td>0 0.4</td>
<td>V</td>
</tr>
<tr>
<td>7.6</td>
<td>OUTPUT LEAKAGE CURRENT HIGH ($I_{LOH}$)</td>
<td>HIGH Z OUTPUT $V_{O} = 5.0$ $V_{cc} = 5.25$</td>
<td>-1.0 1.0</td>
<td>uA</td>
</tr>
<tr>
<td>7.7</td>
<td>OUTPUT LEAKAGE CURRENT LOW ($I_{LOL}$)</td>
<td>HIGH Z OUTPUT $V_{O} = 0.0$ $V_{cc} = 5.25$</td>
<td>-1.0 1.0</td>
<td>uA</td>
</tr>
<tr>
<td>7.8</td>
<td>POWER SUPPLY CURRENT ($I_{CC}$)</td>
<td>$V_{cc} = 5.25V$ ALL INPUTS $= V_{cc}$ DEVICE IS ACTIVE</td>
<td>14</td>
<td>mA</td>
</tr>
<tr>
<td>7.9</td>
<td>BREAKDOWN VOLTAGE ($B_{v}$)</td>
<td>$I_{in} = 10\mu A$, ALL OTHER=OV; TEST ALL INPUTS ONE AT A TIME</td>
<td>7</td>
<td>V</td>
</tr>
</tbody>
</table>
8.0 DYNAMIC CHARACTERISTICS

Unless otherwise specified:

a. $0^\circ \leq T_a \leq 70^\circ C$.
b. $4.75 \leq V_{cc} \leq 5.25$
c. All waveforms and dynamic parameters tested at 1 std TTL load/50pF.
d. Ref dynamic test set up sec 10.0.

tab:

<table>
<thead>
<tr>
<th>ITEM</th>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>Input to Output Prop. Delay Except BREAD</td>
<td>$t_{PHL}, t_{PLH}$</td>
<td>35</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>8.2</td>
<td>Width of Clock High Low</td>
<td>$t_w$</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

e. Ref. timing diagrams Section 9.2

9.0 DYNAMIC TEST WAVEFORMS

9.1 TIMING DEFINITIONS

a. Rise and Fall times are measured at 10 to 90% of the waveform maximum amplitude.
b. Applied waveform specifications:
   $t_r = t_f \leq 9\,\text{ns} \pm 10\%$
c. All waveforms tested at 1 std TTL load/50pF.
9.2 **TIMING DIAGRAMS**

**WAVEFORM FOR INVERTING OUTPUTS**

\[ V_{IN} \rightarrow V_M \rightarrow V_{OUT} \]

\[ V_{IN} \rightarrow V_{PHL} \rightarrow V_{PLH} \]

**WAVEFORM FOR NON-INVERTING OUTPUTS**

\[ V_{IN} \rightarrow V_{M} \rightarrow V_{OUT} \]

\[ V_{IN} \rightarrow V_{PHL} \rightarrow V_{PLH} \]
10.0 DYNAMIC TEST SET-UP

10.1 LOAD CIRCUIT FOR OUTPUT PINS (or equiv. 1 std TTL load/50pF)

Where: \( C_L = 50\text{pF} \)
\( R_L = 2K \)
\( D = 1N916, 1N3064 \) or equivalent

10.2 Input Pulse Definitions

Where: \( V_m = 1.5\text{V} \)
Amplitude = 3.0V
\( t_w = 50\text{ns} \)
Repetition rate = 10mhz
11.0 LOGIC EQUATIONS

GATE ARRAY "B" 40 PIN PLASTIC ("CARMEN")

INPUT DEFINITIONS: ("/" DENOTES ACTIVE LOW INPUT)

***** ALL INPUTS ARE DEFINED AS SEEN AT THE INPUT PAD *****

INPUT WITH "*" DENOTES DC LEVEL SIGNALS, WHICH ARE SET DURING PREVIOUS CYCLE.

+5V
GND
A8, A9, A10, A11, A12, A13, A14, A15
/REF
* ROMEN
* BASICEN
* /INTMPE
* RD4, RD5
* MAP
* /HANDLER
CLK2
/DICFRD
/ACAIIRQ
* DISKBUSY
/SC02ARQ
READ(/WRITE)
/EXTSSEL

TOTAL INPUT PIN COUNT:

+5V, POWER SUPPLY
GND, VSS
A8, A9, A10, A11, A12, A13, A14, A15, ADDRESS BUS
/REF, /REFRESH
* ROM ENABLE
* BASIC ENABLE
* /MATH PAK ENABLE
* CARTRIDGE SELECT
* SELF TEST ENABLE
* PBI HANDLER /CS
CLK2, CPU PHASE 2 CLOCK
/DICFRD/READ
/ACAIIRQ, /ACIA INTERRUPT REQUEST
* DISKBUSY, DISK CONTROLLER BUSY
/SC02ARQ, /SC02 ATTENTION REQUEST
READ(/WRITE), CPU READ(/WRITE)
/EXTSSEL, PBI EXTERNAL SELECT

*** 25 ***
OUTPUT DEFINITIONS: (**/"** DENOTES ACTIVE LOW OUTPUT)

****** ALL OUTPUTS ARE DEFINED AS SEEN AT THE OUTPUT PAD ******
****** ACTIVE LOW OUTPUTS ARE INVERTED BEFORE GOING TO PAD ******

/S4= A15*/A14*/A13*/RD4*/REF  8000H-9FFFH, CARTRIDGE
/S5= A15*/A14*/A13*/RD5*/REF  A000H-BFFFH, CARTRIDGE
/BASIC= A15*/A14*/A13*/RD5*/REF*BASICEN  A000H-BFFFH, BASIC
/OS= ROMEN*A15*/A14*/A13*/A12*/REF  E000H-FFFFF, OS
+ROMEN*A15*/A14*/A13*/A12*/A11*/INTMPE*/REF  C000H-CFFFFH, OS
+ROMEN*/A15*/A14*/A13*/A12*/A11*/MAP*/REF  D800H-DFFFFH, OS MATHPAK
/CCNTL= A15*/A14*/A13*/A12*/A11*/A10*/A9*/A8*/REF  5000H-57FFFH, OS SELFST
/PIA= A15*/A14*/A13*/A12*/A11*/A10*/A9*/A8*/REF  D5XXH, CARTRIDGE CRNL
/POKEY= A15*/A14*/A13*/A12*/A11*/A10*/A9*/A8*/REF  D3XXH, PIA CS
/GTIA= A15*/A14*/A13*/A12*/A11*/A10*/A9*/A8*/REF  D2XXH, POKEY CS

/REMINH= S4  SD4, CARTRIDGE
/EXTENB= +S5  SS5, CARTRIDGE
+BASIC  BASIC (BASIC CS)
+OS  OS (CS)
+REF  REFRESH
+HANDLER  PBI HANDLER
+MILY*/A15*/A13*/A12*/A11*/A10*/A9*/REF  DU00H-D3FFFH, I/O SPACE
+MILY*/A15*/A13*/A12*/A11*/A10*/A9*/REF  DU40H-D5FFFH, I/O SPACE

/DBUSEN= POKEY*CLK2  POKEY CS
+PIA*CLK2  PIA CS
+BASIC*CLK2  BASIC CS
+HANDLER*CLK2  PBI HANDLER CS
+OS*CLK2  OS CS
+S4*CLK2  S4, CARTRIDGE
+S5*CLK2  SS5, CARTRIDGE
+CCNTL*CLK2  CARTRIDGE CONTROL

(IF /D1CFRD = 1)DO= HIGHZ  TRI-STATED OUTPUT
(IF /D1CFRD = 0)DO= DISKBUSY  LOGIC OUTPUT
(IF /D1CFRD = 1)D1= HIGHZ  TRI-STATED OUTPUT
(IF /D1CFRD = 0)D1= ACIAIRQ  LOGIC OUTPUT
(IF /D1CFRD = 1)D7= HIGHZ  TRI-STATED OUTPUT
(IF /D1CFRD = 0)D7= /SCO2ARQ  LOGIC OUTPUT

BREAD(/WRITE)= READ(/WRITE)

/PB1DATEN= A15*/A14*/A13*/A12*/A11*/A10*/A9*/A8*/REF*CLK2  D1XXH
+EXTSEL*CLK2  /EXTSEL TRUE
+/READ

TOTAL OUTPUT PIN COUNT:  *** 15 ***
TOTAL PIN COUNT FOR GATE ARRAY "B":  *** 40 ***
12.0 ELECTRICAL CHARACTERIZATION TESTING

Characterization and device performance tests are to be done on a Sentry 7 with high voltage test heads.
## PIN ASSIGNMENT

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>/HANDLER</td>
</tr>
<tr>
<td>2</td>
<td>CLK2</td>
</tr>
<tr>
<td>3</td>
<td>/EXTSEL</td>
</tr>
<tr>
<td>4</td>
<td>BREAD</td>
</tr>
<tr>
<td>5</td>
<td>READ</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
</tr>
<tr>
<td>7</td>
<td>VSS</td>
</tr>
<tr>
<td>8</td>
<td>/RAMINH</td>
</tr>
<tr>
<td>9</td>
<td>/DBUSEN</td>
</tr>
<tr>
<td>10</td>
<td>/PBIDATEN</td>
</tr>
<tr>
<td>11</td>
<td>D0</td>
</tr>
<tr>
<td>12</td>
<td>DISKBUSY</td>
</tr>
<tr>
<td>13</td>
<td>D1</td>
</tr>
<tr>
<td>14</td>
<td>/ACIAIRQ</td>
</tr>
<tr>
<td>15</td>
<td>/D1CFRD</td>
</tr>
<tr>
<td>16</td>
<td>D7</td>
</tr>
<tr>
<td>17</td>
<td>/SC02ARQ</td>
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<tr>
<td>18</td>
<td>/CCNTL</td>
</tr>
<tr>
<td>19</td>
<td>/PIA</td>
</tr>
<tr>
<td>20</td>
<td>/POKEY</td>
</tr>
<tr>
<td>21</td>
<td>/GTIA</td>
</tr>
<tr>
<td>22</td>
<td>ROMEN</td>
</tr>
<tr>
<td>23</td>
<td>A8</td>
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<tr>
<td>24</td>
<td>A9</td>
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<td>25</td>
<td>A10</td>
</tr>
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<td>26</td>
<td>A11</td>
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<td>28</td>
<td>A13</td>
</tr>
<tr>
<td>29</td>
<td>A14</td>
</tr>
<tr>
<td>30</td>
<td>A15</td>
</tr>
<tr>
<td>31</td>
<td>/OS</td>
</tr>
<tr>
<td>32</td>
<td>MAP</td>
</tr>
<tr>
<td>33</td>
<td>RD5</td>
</tr>
<tr>
<td>34</td>
<td>RD4</td>
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<tr>
<td>35</td>
<td>/INTMPE</td>
</tr>
<tr>
<td>36</td>
<td>/S4</td>
</tr>
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<td>37</td>
<td>/S5</td>
</tr>
<tr>
<td>38</td>
<td>BASICEN</td>
</tr>
<tr>
<td>39</td>
<td>/REF</td>
</tr>
<tr>
<td>40</td>
<td>/BASIC</td>
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