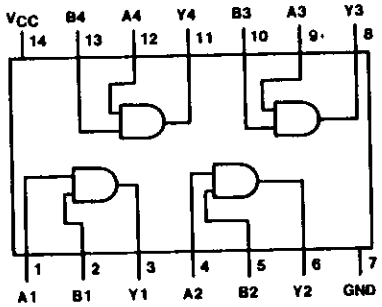
74 S 09 Quad 2-Input AND Gates with Open-Collector Outputs

$Y = AB$



Atari, Inc. 30 E. Plumaria Drive San Jose, CA 95134 A Warner Communications Company	SIZE	DRAWING NO. C025671-001 / REV 1A
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REV	REVISIONS DESCRIPTION	DATE	APPROVED
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Parallel Bus Expansion Memory

Specifications

Steve Miller

11/17/83

C024891-001

ATARI COMPANY CONFIDENTIAL

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NorthWest Design Products Inc.
REORDER NO. 1019A

Parallel Bus Expansion Memory Specfication Rev 2A

1.0 Introduction

This document defines the 48K Memory Expansion Card for the 600XL computer. It will allow the user to expand their computer to a full 64K of RAM making it have the capability of the 800XL computer.

1.1 References

P.B.I. Specfication C061902 S. Miller
Sweet 16 Product Spec C061186 A. Chopra

2.0 Consumer Profile

The typical user will be the first time computer user who, after a small inital investement in a computer, will want to expand into a larger system without an additional expense of buying a second computer system. Using this option we now have a path for a person to grow with his "starter system" to a advance home computer system. This expansion card gives the capability of the existing 800XL. Further addition of the Expansion Box will allow upgrages to a advanced tool for modern times.

3.0 Mechanical Design

The Parallel Bus Memory Expansion should have the XL-series styling and fit in back of the 600XL computer flush with the table top. The unit will also include room for a RFI sheild.

3.1 Dimensions

Lenght	7.31 inches
Depth	4.19 inches
Height	1.63 inches
Weight	2.5 lbs.

4.0 Electrical Design

The Memory Expansion should contain enough memory to allow expansion of the 600XL to 64K. It should also meet the timing requirements of the P.B.I. In addition, it will also provide an interface to the Expansion Box in the rear of the unit. The interface will contain all the signals of the P.B.I. except reserved and power (+5VDC).

Power for the unit will be supplied by the 600XL computer. This includes all interface logic and the RAM.

Shown in Figure 1 are the signals used in the Memory Expansion Device. A brief description follows. Not all the signals are used for the expansion ram but are included for completeness.

	GND	1	2	EXTSEL'
	AØ	3	4	A1
	A2	5	6	A3
	A4	7	8	A5
	A6	9	1Ø	GND
	A7	11	12	A8
	A9	13	14	A1Ø
	A11	15	16	A12
	A13	17	18	A14
	GND	19	2Ø	A15
	DØ	21	22	D1
	D2	23	24	D3
	D4	25	26	D5
	D6	27	28	D7
CONSOLE TOP	GND	29	3Ø	GND CONSOLE BOTTOM
	BØ2	31	32	GND
	Reserved	33	34	RST'
	IRQ'	35	36	RDY
	Reserved	37	38	EXTENB
	Reserved	39	4Ø	REF'
	CAS'	41	42	GND
	MPD'	43	44	RAS'
	GND	45	46	LR/W'
	Reserved	47	48	Reserved
	AUDIO	49	5Ø	GND

Figure 1 PBI Connector
(Looking out of the Computer from the Inside)

4.1 Signals

Shown in figure 1 is the pin-out of the connector looking out of the computer. The signal names and functions are described below.

Pin 2	EXTSEL'	External Select (Input) ==> This open collector line is generated internally by the Parallel Bus Device (PBD). This signal should be active low whenever EXTENB is active and the PBD is selected and there is a valid PBD address on the bus. EXSEL' causes a CAS' inhibit on the main board allowing a remapping process. Although PBD can be mapped in any VALID RAM location, these devices should follow the ATARI guidelines for PBD locations so future ATARI devices can be used. The drive device should be capable of sinking 5 mA.
Pin 3	AØ	Address Line Ø (Output) ==> Address line Ø is a unbuffered output from the microprocessor.
Pin 4	A1	Address Line 1 (Output) ==> Address line 1 is a unbuffered output from the microprocessor.
Pin 5	A2	Address Line 2 (Output) ==> Address line 2 is a unbuffered output from the microprocessor.
Pin 6	A3	Address Line 3 (Output) ==> Address line 3 is a unbuffered output from the microprocessor.
Pin 7	A4	Address Line 4 (Output) ==> Address line 4 is a unbuffered output from the microprocessor.
Pin 8	A5	Address Line 5 (Output) ==> Address line 5 is a unbuffered output from the microprocessor.
Pin 9	A6	Address Line 6 (Output) ==> Address line 6 is a unbuffered output from the microprocessor.
Pin 11	A7	Address Line 7 (Output) ==> Address line 7 is a unbuffered output from the microprocessor.

Pin 12	A8	Address Line 8 (Output) ==> Address line 8 is a unbuffered output from the microprocessor.
Pin 13	A9	Address Line 9 (Output) ==> Address line 9 is a unbuffered output from the microprocessor.
Pin 14	A1Ø	Address Line 1Ø (Output) ==> Address line 1Ø is a unbuffered output from the microprocessor.
Pin 15	A11	Address Line 11 (Output) ==> Address line 11 is a unbuffered output from the microprocessor.
Pin 16	A12	Address Line 12 (Output) ==> Address line 12 is a unbuffered output from the microprocessor.
Pin 17	A13	Address Line 13 (Output) ==> Address line 13 is a unbuffered output from the microprocessor.
Pin 18	A14	Address Line 14 (Output) ==> Address line 14 is a unbuffered output from the microprocessor.
Pin 2Ø	A15	Address Line 15 (Output) ==> Address line 15 is a unbuffered output from the microprocessor.
Pin 21	DØ	Data Line Ø (Bi-directional) ==> Data line Ø is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 22	D1	Data Line 1 (Bi-directional) ==> Data line 1 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 23	D2	Data Line 2 (Bi-directional) ==> Data line 2 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 24	D3	Data Line 3 (Bi-directional) ==> Data line 3 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.

Pin 25	D4	Data Line 4 (Bi-directional) ==> Data line 4 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 26	D5	Data Line 5 (Bi-directional) ==> Data line 5 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 27	D6	Data Line 6 (Bi-directional) ==> Data line 6 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 28	D7	Data Line 7 (Bi-directional) ==> Data line 7 is a buffered line in the 12XX models and unbuffered in the 6ØØ and 8ØØ computers.
Pin 31	BØ2	Buffered Phase 2 Clock (Output) ==> This clock output line is a buffered phase 2 clock from the processor.
Pin 34	RST'	Reset (Output) ==> Reset is a active low signal which occurs either on power-up or by depressing the reset key.
Pin 35	IRQ'	Interrupt Request (Input) ==> This open collector line creates a interrupt on the microprocessor. The interrupt can then invoke the handler ROM or other service routines for the PBD. The driving device should be capable of sinking 5 mA.
Pin 36	RDY	Ready (Input) ==> This open collector input signal allows the PBD to halt the microprocessor ONLY during read cycles. This will extend the read cycle for slow peripherals. The driving device should be capable of sinking 5 mA.
Pin 38	EXTENB	External Decoder Enable (Output) ==> This output goes high when there is a valid RAM access. Any PBD can map during a valid EXTENB but the PBD should only map in according to ATARI specified address locations.

Pin 4Ø	REF'	Refresh (Output) ==>This output can be for refresh timing on voltile memories connected to the PBI.
Pin 41	CAS'	Column Address Strobe (Output) ==> This output can be used for access of DRAM external to the computer. Due to timing restrictions caution should be taken when using this signal in the expansion box.
Pin 43	MPD'	Math Pack Disable (Input) ==> This open collector input is used to disable the math pack section of the OS ROM (D8ØØH-DFFFH). This should be done when the PBD is selected and has a handler resident. The driving device should be capable of sinking 5 mA.
Pin 44	RAS'	Row Address Strobe (Output) ==> This output can be used for access of DRAM external to the computer. Due to timing restrictions caution should be taken when using this signal in the expansion box.
Pin 46	LRØW'	Latched Read Write (Output) ==> This output is active high for a read cycle and active low for a write cycle.
Pin 49	AUDIO	Audio In (Input) ==> This line is tied directly to the audio summation network of the computer. The audio signal input is 1ØØ mV peak to peak with 4.7K ohm source impedance.

Pins 1,1Ø,19,29,3Ø,32,42,45,5Ø	GND
Pins 47,48	+5 VDC
Pins 33,37,39	Reserved

5.0 Product Performance

This section will specify the projected performance of the Memory Expansion. The enviromental and reliablity information is included is targeted from th e sweet 16 sepecfication.

5.1 Enviromental

Operating Enviroment

Temperature =	
Maximum:	45 degrees C
Minimum:	10 degrees C
Humidity =	
Maximum:	90% R.H. (Non Condensing)
Minimum:	15% R.H.
Altitude =	
Maximum:	3000 Meters (9840 feet) (720 millibars)
Minimum:	-60 Meters (-197 feet) below sea level

Non-Operating Enviroment

Temperature =	
Maximum:	60 degrees C
Minimum:	30 degrees C
Humidity =	
Maximum:	90% R.H. Should condensing occur unit
Minimum:	0% R.H. must be dried off before operation
Altitude =	
Same as operating	

5.2 Endurance Levels

ESD Susceptiablity

No product damage or data loss with 10KV to 20KV discharge at any point accessible to the user except the connectors with 65% RH.

Vibration

Operation:	.1g ± 10% 5 to 500Hz
Resonance Search:	Sine scan 5-100 Hz dwell on resonances 1.0g for 10 minutes.

Transportation:	100 to 300 cycles per minute 2 directions 90 degrees apart, 30 minutes; each frequency to be such as to raise package from the table 0.06 in., acceleration to be 1.0g (min) No Damage should result.
Impact Test:	Free fall distance of 24 in. on corner, edge, and all 6 faces. No damage should occur to a packed unit.
Ramdom Vibration:	0.04g 2Hz 15minutes; 10 to 1000Hz 6.3g RMS
Termal Shock:	10 degrees C for 3 hours power on raise temperature, 5 degrees per minute to 45 degrees C for 5 hours power off drop temperature 5 degrees C per minute to 10 degrees C. Repeat cycle 5 times no damage.

5.3 MTBF & MTTR

The targeted MTBF for the Memory Expansion is 8000 hours continous power-on at 25 degrees C.

The targeted MTTR for the unit is 5 minutes.

5.4 Compliances

UL 114 & UL 94HB
CSA C22.2 No. 154
FCC Docket 20780, Part 15, Subpart J, Class B