Symptoms exhibited by version 2 AMY chips.

1. At vcc=5.0 volts the audio output picked up spiky noise as the clock rate was increased above 4 or 5 MHz. The chip is designed to operate at 8MHz. Increasing vcc increased the operating speed for each individual chip. Moving the clock rate up and down did not seem to change the logical operation of the chip.

2. Occasionally, about 10% of the time, a single command sent to the chip resulted in two operations taking place. Usually this was seen as a second harmonic being turned on when another was intentionally turned on or off.

3. When any last harmonic pair flag was set the audio output almost dissappeared and was at most a tiny sawtooth waveform that seemed to have no relationship to the requested parameters.

Physical experiments

1. Sam Nicolino probed unpassivated chips extensively and verified proper operation of most of the control logic. He expressed some concern that the non-overlap of clk and clkn was not as clean as he would like but was probably adequate.

2. Setting some lhp flags (to get multiple voices) and then sending one of the voices on a long frequency ramp allowed us to read out the current value of the frequency and verify that it was ramping ok. This seemed to indicate that the voice RAM was functioning ok.

3. When probing the phase RAM, Ben and I discovered that loading th output of the second inverter for the lsb of the address caused the chip to "work" in the multivoice mode. In this mode, however, the harmonics of voice 1 were in fact harmonics of the fundamental of voice 0. Similarly, every odd numbered voice tracked with the frequency selected for the next lower numbered voice. The fundamental frequencies of the odd numbered voices had no effect. We hypothesized that the phases of odd numbered voices were being overwritten by those of the even numbered voices. To test this we observed the memory data emerging from the phase RAM. After each address change the phase update (frequency) is added to the running value and the sum is written back. What we saw was that no change in the memory data occurred at the address change when the lsb went high but an update was written back. The conclusion we drew was that selecting RAM cells onto bit lines that were not adequately charged was causing the cells to flip to agree with the previous data on the bit lines. By loading the address decoder assymetrically we were introducing significant contention during the even-to-odd change but also introducing a nice non-overlap region during the odd-to-even transition. There is, of course, never a transition in the one voice operation, hence no contention and the phase advances correctly.

Sections of the chip which are involved in the signal formation have not been reviewed at the same level of detail. The effort has been concentrated on the control section of the chip because the envelope and sine wave generation of the devices appear to work perfectly and a small error should not have significant impact if not discovered until later.

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1) Abbreviated History
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The SILOS input net list used for the simulation was extracted from Daisy drawings in about August 1984 with a program written by Bob Hemming in "Daisy Modeling Language". (The extraction program has since dissappeared). Some modifications were made in the Daisy drawings after the net list was extracted. The Daisy drawings represented a manual redesign of the TTL breadboard (which runs well) into gates suitable for use in an NMOS integrated circuit. The drawings were then used as the basis for manual layout of the chip using a CALMA design system and a library of cell designs.

The CALMA layout was processed by several error checking programs purchased from NCA Corporation and the warning messages were each checked by an engineer to verify that it was a false alarm due to inadequacies in the checking programs. Programs were not available until recently to compare the circuit laid out in silicon against the netlist extracted from the Daisy drawings. (Such a check is in progress now.) A computer tape with the layout was transmitted to NCR in September and version 1 parts were received in October. Failure of these parts was diagnosed as a timing problem in the command register section and a mistake in the polarity of a ROM address line in the sine and exponential ROMs (both base and slope sections of each).

Fixes were made in the layout and no further design rule check was made before the second layout tape was sent to NCR in November. (False confidence and an attempt to be ready for the January CES lead us to opt for a quick turn-around.) Version 2 parts were received in late December after the principal engineer, Sam Nicolino, had left the company. Version 2 parts generated excellent audio quality but failed to respond reliably to commands from the host processor. They also failed to synthesize multiple voices (even unreliably) and the audio waveform became noisy at full clock rates. Most of the microprobing and testing discussed below was done on this run of chips.

The chips are about 281 by 203 mils (57,043 square mils) using 3 micron HMOS design rules. At NCR's suggestion version 2 was shrunk by 10% which would yield 252.9 x 182.7 = 46,205. They are packaged in 40 pin carriers, dissipate about one watt and require a single 5 volt supply.

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2) Patches to SILOS input data to make the simulation run but which have no implications for the physical device.
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20. The divide-by-two clock generator on the chip consists of 3 inverters in a ring. SILOS assigns an unknown state to the output of an inverter whose input is unknown thus yielding a stable ring of unknowns. To break this and let the clock run in the simulation I initialized one of the nodes in the ring

21. Network description lines like "xyz .nmos .vcc .vcc abc" were generated by the transistor pullups used in the chip. These were replaced by "abc .res .vcc" since the current version of SILOS interprets the original line as a short circuit to vcc.

22. The SILOS model of a RAM has resistive strength outputs in both the high and low level states. (Whereas nmos gates are modelled with resistive highs and driving strength lows.) This lead to conflicts when/where RAMs were connected to busses with pullups. I have sidestepped this difficulty in the simulator by removing the pullups from the HRAM, VRAM and PHASERAM data busses and installing pullups internally to all tristate drivers connected to those busses. The macro cell definition "TRIHpu" was created and substituted for "TRIH" where needed. Ben Calpo's SPICE simulations indicate that the RAM interface cell used in the chip does have the ability to drive a bus with transistor pullups.

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3) Patches to the SILOS input data which reflect potential problems in the chip even though the chips we have now do not exhibit these problems.

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30. A special version of the counter cell was inserted into the SILOS net list for the least significant bit of the voice counter. With the cell really present in the silicon the SILOS simulation enters into an oscillation with the feedback used to stop the voice counter at its maximum value. One chip was microprobed and the oscillation was not present (at least while the probe was loading the circuit). Furthermore no change was heard in the audio output when the probe contacted the chip and we have no observed problems that seem related to such hypothetical oscillations.

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4) Logic changes to make the chip testable.

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40. A mistake was discovered in the Daisy drawings and the layout which connected a preset in the clock generator to ground instead of vcc.

41. On version 2 the clock decoder holds the system in phase P1 during reset and the first clock cycle after reset becomes inactive is also P1. One ramification is that garbage is written into phase RAM location 0 (instead of clearing it). This probably would not degrade the music but it will make the output unpredictable and hence testing will be more difficult.

42. A reset was added to the ZEROB flipflop.

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5) Logic changes necessary to make the chip usable.

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50. Commands from the host processor must be synchronized with the internal uses of the chip's bus to avoid the malfunction observed in version 2. This is accomplished by adding some gates and a delay latch.

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6) Electrical (as opposed to logical) changes needed to operate at full speed and within the design rules required for good yield.

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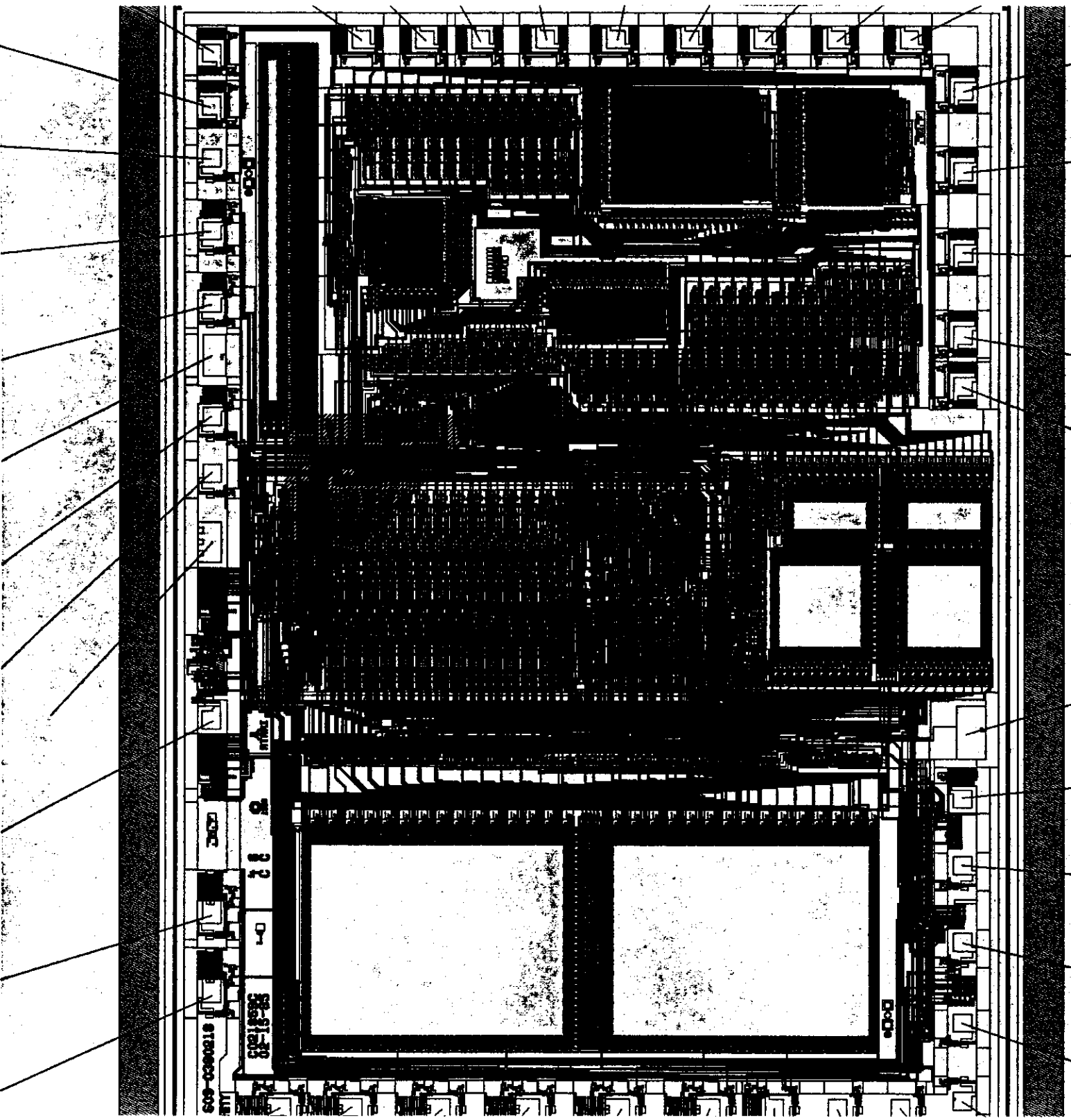
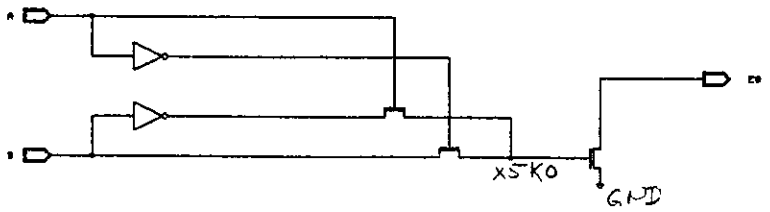
60. The distribution of certain signals, notably precharge, was thru very long polysilicon runs. This lead to poor rise times at the load locations and potentially insufficient levels at full clock speed. Several edits have been made in the layout to alleviate this situation. Ben has checked and found no remaining runs long enough to cause problems.

61. Some enhancement implants of pulldowns were deleted from the ROMs of the chip in versions 1 and 2 due to an error in a program that automatically generated the layer 9 mask. A checking program eventually pointed out the problem and it has been corrected. This is probably the reason that the audio waveforms "break up" at full clock frequency. No missing implants of pulldowns were found in locations other than the lookup ROMs.

62. The signal T10MHZ was buffered. This was required for the synchronization of the "load command" signal and the external reset signal across process parameters, temperature, voltage and input clock duty cycle.

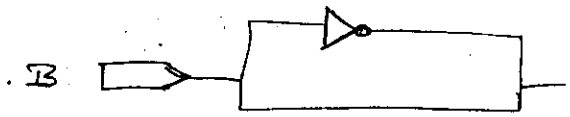
63. The output of the cross-coupled nors generating the non-overlapping clocks to the CLK, CLKN and PRECH buffers was buffered. This was done to make the divide-by-two and PRECH clock generator circuits less sensitive to the effects of input clock duty cycle at high clock frequencies.



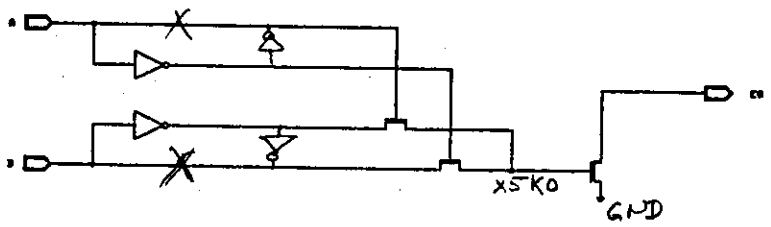


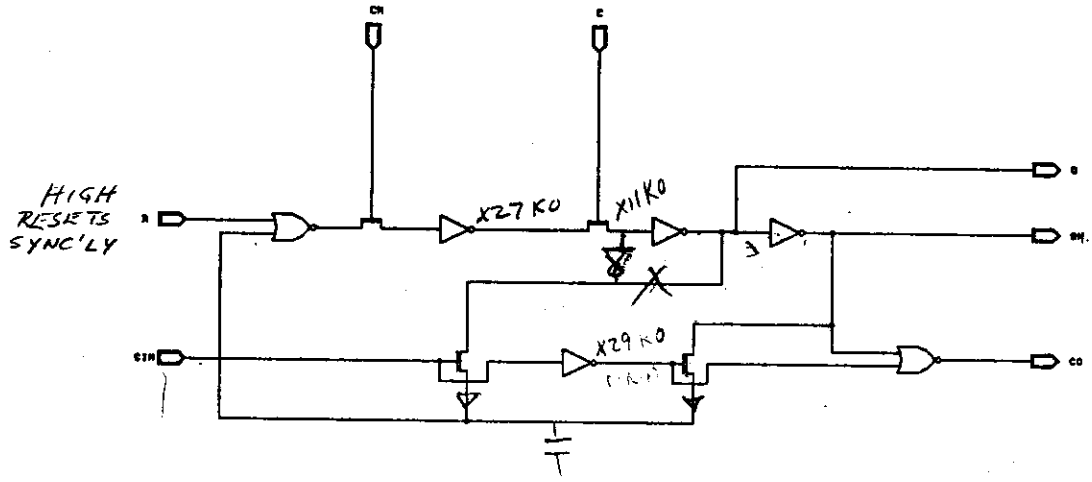
ORIGINAL

Problem: If A is unknown then SILOS models both transistors as ON and result is unknown.

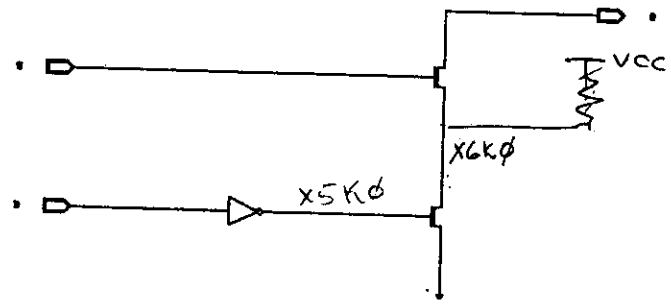


Patch:





NOTES:	ATARI A.S.G.
KAKU/BERGIO	
DATE: 8/9/83	ANY - CNTR CELL
DATE: 6/20/84	
DATE: 7-18-84 BP	
	SHEET 36 OF 52 REV A



NOTES:	ATARI A.S.G.
KAKU/BERGIO	
DATE: 8/9/83	ANY - TRIM CELL
DATE: 6/20/84	
DATE: 7-18-84 BP	
	SHEET 39 OF 52 REV A