REV	REVISIONS DESCRIPTION	DATE	APPROVED
3	ENG REL PER ERC# EQ2494P	4/3/84	[illegible]
4	INCORPORATED PER ERC EO481	4/4/84	[illegible]

ENGINEERING RELEASED

	1450XLD	
NEXT ASSY	USED ON	

DRAWN BY / DATE: D. Alvitre 3/20/84

CHECKED: [illegible] Hoopai 3/20/84

ENGINEER: [illegible] Hoopai 3/20/84

APPROVED: [illegible] 3/29/84

APPROVED: [illegible] 4/2/84

ATARI®

Atari, Inc.
30 E. Plumaria Drive
San Jose, CA 95134
A Warner Communications Company

TITLE: GATE ARRAY "CARMEN"

SIZE	DRAWING NO.	REV
A	C025338-001	4

SCALE

SHEET 1 OF 14

INDEX

1.0 SCOPE

This document is a preliminary specification of the electrical and mechanical requirements for a 40 pin custom high speed CMOS gate array I.C. device designated for use on the "TONG" project. The device is currently under development and there may be revisions to this document before it is Production Released.

2.0 APPLICABLE DOCUMENTS

The following documents, at the revision which is in effect on the date of the Purchase Order, shall form part of this specification to the extent referenced herein.

a. CO99901 - Qualification and Reliability Requirements for Integrated Circuits and Discrete Semiconductors.
b. CO99902 - Handling of Devices Susceptible to Static Discharge.
c. CO99905 - External Visual and Solderability Requirements.
d. CO99906 - Internal Visual Requirements for Atari Semiconductors.
e. CO21538 - Electrostatic Discharge Sensitivity Testing.
f. CO99931 - Dual In-Line Package, General Specifications.

3.0 DEVIATIONS

Product sold to Atari, Inc. under this specification must be identical to original approved samples. Any changes to the product must receive Atari, Inc. sample reapproval prior to delivery. Any deviation from this specification, or from any of the above listed applicable documents, must be approved in writing through the current Atari Deviation Procedure prior to any deviation taking place.

4.0 PRECEDENCE

This specification, including all approved deviations, shall be the governing document for device acceptance. In the event of conflict between this document and any other document, contract, specification or requirement, the manufacturer is responsible to notify Atari, Inc. for written disposition from the affected functional group(s), as identified within this document.

5.0 GENERAL REQUIREMENTS

5.1 ELECTROSTATIC DISCHARGE

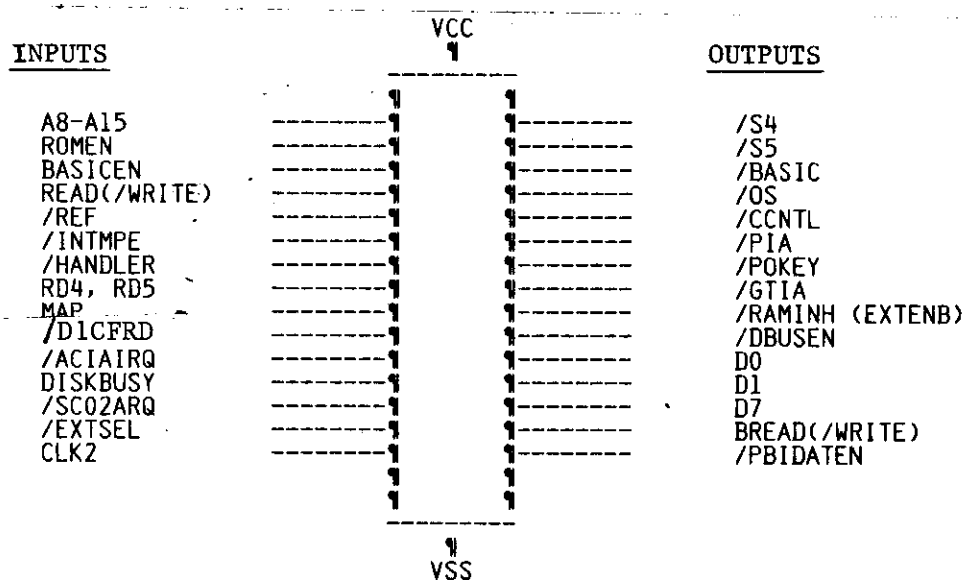
Parts must conform to the requirements of the Atari, Inc. Specification #CO21538, Electrostatic Discharge Sensitivity Testing.

5.2 MARKING

Minimally, parts must be marked permanently and legibly as per Atari, Inc. Specification #C099901 para. 10.1.12 with:

a. Atari Part Number
b. Date Code
c. Copyright Symbol and information:
   - © ATARI (Year); year must be represented as either the full year (e.g. 1983) or the last two digits (e.g. 83)
d. Vendor or industry recognized identification symbol
e. Pin #1 Identification

5.3 BLOCK DIAGRAM

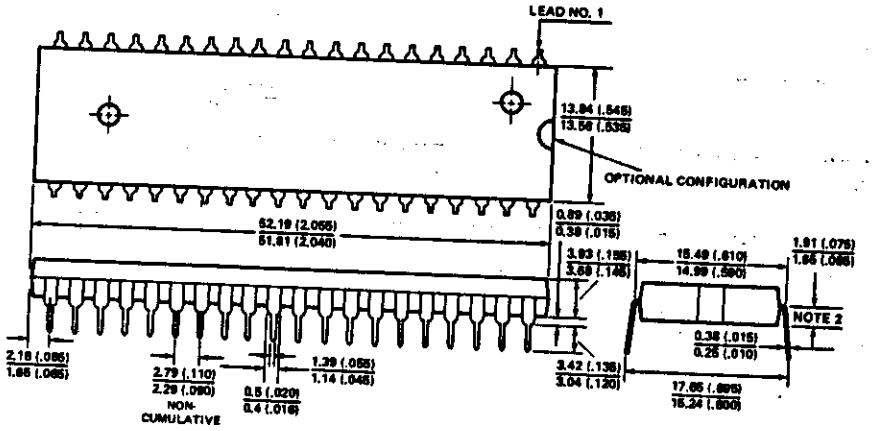


NOTE: See Section 13.0 for pin assignment.

5.4 PACKAGE DESCRIPTION

Package shall be void-free plastic.

N PACKAGE — PLASTIC
(40-PIN)



5.5 LEAD INTEGRITY AND SOLDERABILITY

As per Atari, Inc. Specification #C099901, para. 10.1.11 Lead Integrity and 10.1.16 Solderability.

6.0 ABSOLUTE MAXIMUM RATINGS

Limits beyond which the life of the part may be impaired. It is NOT implied that the device should be operated at these limits. If the part is operated at or near these limits, applicable manufacturers' derating calculations must be imposed.

ITEM	CHARACTERISTIC	LIMITS	UNITS
6.1	SUPPLY VOLTAGE Vcc TO GND (Vcc)	-0.5 TO +7.0	V
6.2	VOLTAGE APPLIED TO ANY INPUT (Vai)	-0.5 TO +7.0	V
6.3	VOLTAGE APPLIED TO ANY OUTPUT (Vao)	-0.5 TO +7.0	V
6.4	POWER DISSIPATION (Pd)	75	mW
6.5	JUNCTION TEMP. Ta=70° (Tj)	TBD	°C
6.6	OPERATING TEMPERATURE (Ta)	0 TO 70	°C
6.7	STORAGE TEMPERATURE (Tstj)	-55 TO +150	°C

7.0 STATIC CHARACTERISTICS

Unless otherwise specified:

a. $0 \leq Ta \leq 70°C$
b. $4.75 \leq Vcc \leq 5.25$
c. Positive current flows into the device
d. $C_{LOAD} = 50pF$

ITEM	CHARACTERISTICS	CONDITION	LIMITS		UNITS
			min	max	
7.1	INPUT VOLTAGE HIGH (VIH)		2.0	Vcc	V
7.2	INPUT VOLTAGE LOW (VIL)		-0.3	0.8	V
7.3	INPUT CURRENT (I_I)	$0 \leq Vin \leq 5.25$ $Vcc = 5.25$	-10	10	uA
7.4	OUTPUT VOLTAGE HIGH (VOH)	$Vcc = 4.75$ $I_{OH} = -100uA$	2.4	5.0	V
7.5	OUTPUT VOLTAGE LOW (VOL)	$Vcc = 4.75$ $I_{OL} = 1.6$ mA	0	0.4	V
7.6	OUTPUT LEAKAGE CURRENT HIGH (I_{LOH})	HIGH Z OUTPUT $V_O = 5.0$ $Vcc = 5.25$	-1.0	1.0	uA
7.7	OUTPUT LEAKAGE CURRENT LOW (I_{LOL})	HIGH Z OUTPUT $V_O = 0.0$ $Vcc = 5.25$	-1.0	1.0	uA
7.8	POWER SUPPLY CURRENT (I_{CC})	Vcc = 5.25V ALL INPUTS = Vcc DEVICE IS ACTIVE		14	mA
7.9	BREAKDOWN VOLTAGE (Bv)	Iin=10uA, ALL OTHER=0V; TEST ALL INPUTS ONE AT A TIME	7		V

8.0 DYNAMIC CHARACTERISTICS

Unless otherwise specified:

a. $0° \leq Ta \leq 70°C$.
b. $4.75 \leq Vcc \leq 5.25$
c. All waveforms and dynamic parameters tested at 1 std TTL load/50pF.
d. Ref dynamic test set up sec 10.0.

ITEM	PARAMETER	SYMBOL	MIN	MAX	UNIT
8.1	Input to Output Prop. Delay Except BREAD	t_{PHL}, t_{PLH}		35 15	ns ns
8.2	Width of Clock High Low	tw	50 50		ns ns

e. Ref. timing diagrams Section 9.2

9.0 DYNAMIC TEST WAVEFORMS

9.1 TIMING DEFINITIONS

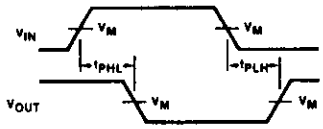
a. Rise and Fall times are measured at 10 to 90% of the waveform maximum amplitude.

b. Applied waveform specifications:
$t_r = t_f \leq 9ns \pm 10\%$

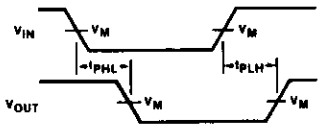
c. All waveforms tested at 1 std TTL load/50pF.

9.2 TIMING DIAGRAMS

WAVEFORM FOR INVERTING OUTPUTS

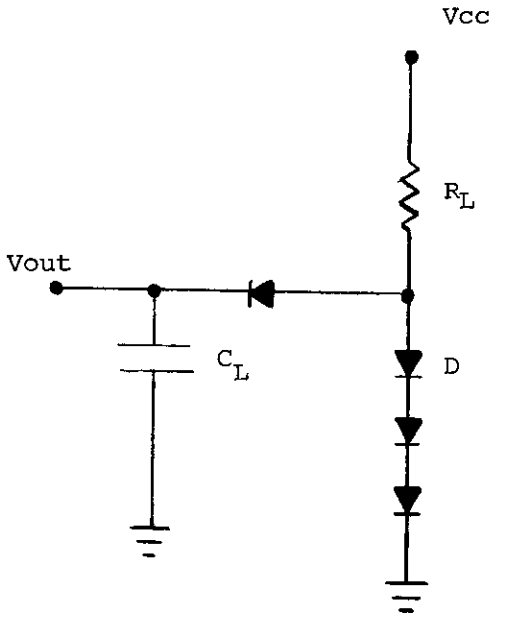


WAVEFORM FOR NON-INVERTING OUTPUTS



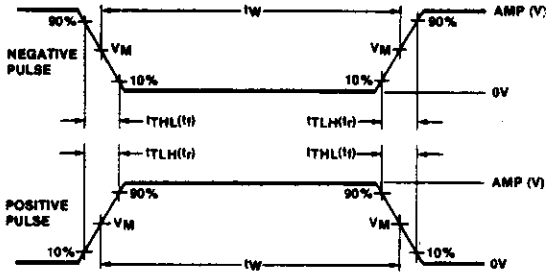
10.0 DYNAMIC TEST SET-UP

10.1 LOAD CIRCUIT FOR OUTPUT PINS (or equiv. 1 std TTL load/50pF)



Where: C_L = 50pF
R_L = 2K
D = 1N916, 1N3064 or equivalent

10.2 Input Pulse Definitions



Where: V_m = 1.5V
Amplitude = 3.0V
tw = 50ns
Repetition rate = 10mhz

11.0 LOGIC EQUATIONS

```
********************************************************************************
GATE ARRAY "B"  40 PIN PLASTIC  ("CARMEN")
--------------------------------------------------------------------------------
INPUT DEFINITIONS:      ("/" DENOTES ACTIVE LOW INPUT)
       ***** ALL INPUTS ARE DEFINED AS SEEN AT THE INPUT PAD *****
INPUT WITH "*" DENOTES DC LEVEL SIGNALS, WHICH ARE SET DURING PREVIOUS CYCLE.
--------------------------------------------------------------------------------
               +5V                                      VCC, POWER SUPPLY
               GND                                      VSS
               A8, A9, A10, A11, A12, A13, A14, A15     ADDRESS BUS
               /REF                                     /REFRESH
*              ROMEN                                    ROM ENABLE
*              BASICEN                                  BASIC ENABLE
*              /INTMPE                                  /MATH PAK ENABLE
*              RD4, RD5                                 CARTRIDGE SELECT
*              MAP                                      SELF TEST ENABLE
*              /HANDLER                                 PBI HANDLER /CS
               CLK2                                     CPU PHASE 2 CLOCK
               /D1CFRD                                  D1CFH/READ
               /ACIAIRQ                                 /ACIA INTERRUPT REQUEST
*              DISKBUSY                                 DISK CONTROLLER BUSY
               /SC02ARQ                                 /SC02 ATTENTION REQUEST
               READ(/WRITE)                             CPU READ(/WRITE)
               /EXTSEL                                  PBI EXTERNAL SELECT
TOTAL INPUT PIN COUNT:                                  *** 25 ***
```

OUTPUT DEFINITIONS: ("/" DENOTES ACTIVE LOW OUTPUT)

***** ALL OUTPUTS ARE DEFINED AS SEEN AT THE OUTPUT PAD *****
***** ACTIVE LOW OUTPUTS ARE INVERTED BEFORE GOING TO PAD *****

/S4=	A15*/A14*/A13*RD4*/REF	8000H-9FFFH, CARTRIDGE
/S5=	A15*/A14*A13*RD5*/REF	A000H-BFFFH, CARTRIDGE
/BASIC=	A15*/A14*A13*/RD5*/REF*BASICEN	A000H-BFFFH, BASIC
/OS=	ROMEN*A15*A14*A13*/REF +ROMEN*A15*A14*/A13*/A12*/REF +ROMEN*A15*A14*/A13*A12*A11*INTMPE*/REF +ROMEN*/A15*A14*/A13*A12*/A11*MAP*/REF	E000H-FFFFH, OS C000H-CFFFH, OS D800H-DFFFH, OS MATHPAK 5000H-57FFH, OS SELFTST
/CCNTL=	A15*A14*/A13*A12*/A11*A10*/A9*A8*/REF	D5XXH, CARTRIDGE CONTRL
/PIA=	A15*A14*/A13*A12*/A11*/A10*A9*A8*/REF	D3XXH, PIA CS
/POKEY=	A15*A14*/A13*A12*/A11*/A10*A9*/A8*/REF	D2XXH, POKEY CS
/GTIA=	A15*A14*/A13*A12*/A11*/A10*/A9*/A8*/REF	D0XXH, GTIA CS
/RAMINH= (EXTENB)	S4 +S5 +BASIC +OS +REF +HANDLER +A15*A14*/A13*A12*/A11*/A10*$\overline{REF}$ +A15*A14*/A13*A12*/A11*A10*/A9*$\overline{REF}$	S4, CARTRIDGE S5, CARTRIDGE BASIC CS OS CS REFRESH PBI HANDLER D000H-D3FFH, I/O SPACE D400H-D5FFH, I/O SPACE
/DBUSEN=	POKEY*CLK2 +PIA*CLK2 +BASIC*CLK2 +HANDLER*CLK2 +OS*CLK2 +S4*CLK2 +S5*CLK2 +CCNTL*CLK2	POKEY CS PIA CS BASIC CS PBI HANDLER CS OS CS S4, CARTRIDGE S5, CARTRIDGE CARTRIDGE CONTROL

(IF /D1CFRD = 1)D0=	HIGHZ	TRI-STATED OUTPUT
(IF /D1CFRD = 0)D0=	DISKBUSY	LOGIC OUTPUT
(IF /D1CFRD = 1)D1=	HIGHZ	TRI-STATED OUTPUT
(IF /D1CFRD = 0)D1=	ACIAIRQ	LOGIC OUTPUT
(IF /D1CFRD = 1)D7=	HIGHZ	TRI-STATED OUTPUT
(IF /D1CFRD = 0)D7=	/SCO2ARQ	LOGIC OUTPUT

BREAD(/WRITE)= READ(/WRITE) BUFFERED READ(/WRITE)

/PBIDATEN=	A15*A14*/A13*A12*/A11*/A10*/A9*A8*/REF*CLK2 +EXTSEL*CLK2 +/READ	D1XXH /EXTSEL TRUE

TOTAL OUTPUT PIN COUNT: *** 15 ***

TOTAL PIN COUNT FOR GATE ARRAY "B": *** 40 ***

12.0 ELECTRICAL CHARACTERIZATION TESTING

Characterization and device performance tests are to be done on a Sentry 7 with high voltage test heads.

13.0 PIN ASSIGNMENT

Pin #	Signal
1	/HANDLER
2	CLK2
3	/EXTSEL
4	BREAD
5	READ
6	VCC
7	VSS
8	/RAMINH
9	/DBUSEN
10	/PBIDATEN
11	D0
12	DISKBUSY
13	D1
14	/ACIAIRQ
15	/D1CFRD
16	D7
17	/SCO2ARQ
18	/CCNTL
19	/PIA
20	/POKEY
21	/GTIA
22	ROMEN
23	A8
24	A9
25	A10
26	A11
27	A12
28	A13
29	A14
30	A15
31	/OS
32	MAP
33	RD5
34	RD4
35	/INTMPE
36	/S4
37	/S5
38	BASICEN
39	/REF
40	/BASIC